## **Introductory Lecture - COA**



S.Venkatesan Network Security and Cryptography Lab Department of Information Technology Indian Institute of Information Technology, Allahabad venkat@iiita.ac.in

1

Acknowledgement: The contents and figures are copied from various sources. Thanks to all authors and sources made those contents public and usable for educational purpose

## COA?



- Architecture: High Level, What a computer should do
  - Instruction set,
  - Number of bits used for data representation,
  - I/O Mechanisms
  - Addressing Techniques
- Organization: Low Level, How a computer do, Interconnection among units
  - Control signals,
  - Interfaces,
  - Memory Technology

## **Functional Block of Computer**



## Performance

- In FLOPs
- Multi-Core
- RAM

Year	Technology	Performance
1951	Vacuum Tube	1
1965	Transistor	35
1975	IC	900
1995	VLSI Circuit	2400000
2005	ULSI Circuit	620000000

CPU Execution Time – User CPU Time and System CPU Time

## Generation

Generations of computers	Generations timeline	Evolving hardware
First generation	1940s-1950s	Vacuum tube based
Second generation	1950s-1960s	Transistor based
Third generation	1960s-1970s	Integrated circuit based
Fourth generation	1970s-present	Microprocessor based
Fifth generation	The present and the future	Artificial intelligence based

## Motherboard



Source: https://turbofuture.com/computers/the-motherboard-components

## Computer processor's speed

- Named after Heinrich Hertz and abbreviated as Hz or illustrated as the f symbol, hertz equals one cycle per second, measuring the waves or frequencies of electric changes each second.
- Hertz is commonly used to measure a computer monitor's refresh rate and a computer processor's speed.

# Amplitude **Heinrich Hertz** (power) ComputerHope.com One oscillation (one cycle or hertz)

Wave Model

#### Concepts of Performance and Speedup



CPU time = Instructions × (Cycles per instruction) × (Secs per cycle) = Instructions × CPI / (Clock rate)

Instruction count, CPI, and clock rate are not completely independent, so improving one by a given factor may not lead to overall execution time improvement by the same factor.

#### Elaboration on the CPU Time Formula

CPU time = Instructions × (Cycles per instruction) × (Secs per cycle) = Instructions × Average CPI / (Clock rate)

- Instructions: Number of instructions executed, not number of instructions in our program (dynamic count)
- Average CPI: Is calculated based on the dynamic instruction mix and knowledge of how many clock cycles are needed to execute various instructions (or instruction classes)
- Clock rate:  $1 \text{ GHz} = 10^9 \text{ cycles / s}$  (cycle time  $10^{-9} \text{ s} = 1 \text{ ns}$ ) 200 MHz = 200 ×  $10^6 \text{ cycles / s}$  (cycle time = 5 ns)



Slide from University of California, Santa Barbara

#### **Dynamic Instruction Count**



Slide from University of California, Santa Barbara

### Processors



Ref: Pranav Tendulkar Mapping and Scheduling on Multi-core Processors using SMT Solvers

# **Processing Units**

<ul> <li>CPU</li> <li>Small models</li> <li>Small datasets</li> <li>Useful for design space exploration</li> </ul>
<ul> <li>GPU</li> <li>Medium-to-large models, datasets</li> <li>Image, video processing</li> <li>Application on CUDA or OpenCL</li> </ul>
<ul> <li>TPU</li> <li>Matrix computations</li> <li>Dense vector processing</li> <li>No custom TensorFlow operations</li> </ul>
<ul> <li>FPGA</li> <li>Large datasets, models</li> <li>Compute intensive applications</li> <li>High performance, high perf./cost ratio</li> </ul>

## Memory Hierarchy



## What happens to your program



FIGURE 1.4 C program compiled into assembly language and then assembled into binary machine language. Although the translation from high-level language to binary machine language is shown in two steps, some compilers cut out the middleman and produce binary machine language directly. These languages and this program are examined in more detail in Chapter 2.

Copyright © 2014 Elsevier Inc. All rights reserved.

# Thank You