Homework Assignment on Arithmetic Circuits

Q1. Using only one 3-bit counter and minimum components listed below, design a counter that generates the following sequence repeatedly:
5->7->9->11->13->15->17->19->5.....

Q2. Design a FSM circuit which has 2-bit input X and an output Y. The output Y becomes 1 if the cumulative sum of the numbers in sequence X is multiple of 3, else it is 0.
For example :
X : 00 -> 11 -> 01 ->10 ->00->01.....
Y : 1 - > 1 -> 0 -> 1 -> 1 -> 0.....

Q3. Use the two's complement system to add the signed numbers 11110010 and 11110011.
Determine, in decimal, the sign and value of each number and their sum.

Q4. Someone claims that if you type "0100" into a file using a standard text editor, you have written 4 bits to the file, and thus created a binary file. Explain what's correct and incorrect about this statement.

Q5. Register A holds binary value 11011001. Determine the **Register B** operand and the logic operation to be performed in order to change the value in **A** to :

i. 01101101 **ii.** 11111101

Q6. In a normal n-bit adder, to find out if an overflow has occurred we make use of _____

Q7. A 4-bit carry lookahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assume that the carry network has been implemented using two-level AND-OR logic and all the inputs are available in both complemented and un-complemented forms. The delay of each gate is assumed to be one time unit,
(i) what is the overall propagation delay of carry look ahead the adder?
(ii) Compare the delay with the delay of the ripple carry adder constructed using same AND, OR, NOT, NAND, NOR gates only

Q8. (a) How many addition and subtraction operations are peformed when 23 is multiplied with -7 using the Booth's multiplication method; both numbers are expressed in 8 bit two's complement format.

(b) Booth's algorithm for integer multiplication gives worst performance when the multiplier pattern is
(i) 101010…..1010 (ii) 100000……0001
(iii) 111111…..1111 (iv) 011111……1110

Choose one of the option and justify your choice.

Q.9. **(a)** Represent the radix-2 booth recoding of -5. Calculate(-5)*(14) using Booth's algorithm.
(b) Use the restoring division algorithm to perform (-7)/3

Q10. NVDIA has a half format, which is similar to IEEE 754 except that it is only 16 bits wide. The left most bit is still sign bit, th exponent is 5 bits wide and stored in excess 16 format and mantissa is 10 bits long. Using the NVDIA format,
find the (i) sum and (ii) product of two decimal numbers :