Homework Set 2

Q1. IIIT student staying in one of the institute hostels has to make up his/her mind about his/her dinner. There can be three situations which may arise :

Situation 1 - If he/she has enough money (M) and at least three of his/her friends (F) also agree to go out for dinner, and it is not raining (R), he/she will have dinner with his/her friends in a restaurant at Civil Lines.

Situation 2 - If he/she is not able to go out, but at least three of his/her friends agree to join him/her (J), if the kind of food he/she wanted is available on home delivery (K) he/she will order home delivery of food from online food delivery services, *Swiggy* maybe.

Situation 3 - But, if the general feeling is that the food in the hostel mess is good on that day (G), he/she will have his/her dinner in the hostel mess.

Let his/her decision be denoted by a 2-bit output D_1D_0:
D_1D_0= 00 : He/She eats in the hostel mess,
D_1D_0= 01 : He/She goes out to have dinner in a restaurant, and D_1D_0= 10 : He/She orders food through home delivery app.

Assign binary variables to represent the three situations using the letters indicated in parentheses above, and obtain both POS expressions for D_1 and D_0 in terms of these variables, simplifying the expressions as far as possible.

Q2. An economist proposed the following technique for making money in the stock market:
1. If the dividends paid on the stock exceed those paid on a bond, buy the stock.
2. If the dividends paid on the bond exceed those paid on a stock, buy the bond unless the growth rate of the stock has been at least 25% annually for the past 5 years, in which case the stock should be purchased.

Design a circuit with NAND gates to give two outputs one going high for buying the stock and the other going high for buying the bond.

Q3. Buses leave the terminal every hour on the hour unless there are fewer than 10 passengers or the driver is late. If there are fewer than 10 passengers the bus will wait for 10 minutes or the number of passengers increases to 10. If the bus leaves on time it can travel at 60kmph. If the bus leaves late or if it rains the bus can travel only at 30kmph. Under what condition will the bus travel at 60kmph? Construct a circuit to get an output 1 for the bus to travel at 60kmph using NAND gates.

Q4. In an examination consisting of three papers A, B and C, a student can pass (i) if he/she gets 60% marks in at least one of them and more than 50% in the rest, (ii) if he/she gets 60% marks in two of them and greater than 40% in the third, (iii) if he/she gets greater than 80% in one of them and greater than 40% in one of the other two and greater than 35% in the other. Realize the logic using basic gates to get an out put 1 when the student passes the examination.

Q5. A combinational circuit has to perform the operation z = x (y + 2), where both x and y are integers, x lying in the range 1 3 and y lying in the range 0-3. Let x and y be represented by 2-bit binary codes $\mathbf{X_1X_0}$ and $\mathbf{Y_1Y_0}$ respectively, the output z being represented by the four-bit binary code $\mathbf{Z_3Z_2Z_1Z_0}$.

(a) Construct four K-maps for the output variables $\mathbf{Z_3Z_2Z_1Z_0}$ in the format given below, treating the undefined combinations of $\mathbf{X_1X_0}$ as "don't care".
(b) Hence obtain the Boolean expressions for $\mathbf{Z_3Z_2Z_1Z_0}$ in the minimal SOP form.
Assuming Quad 2-input and Dual 4-input gate chips to be available, find out the number of different types of gates required and hence the chip count for a two-level NAND-NAND realisation.

Q6. Design a counter that counts in the sequence: 101, 100, 011, 010, 001, 000, 101, ...

Implement a circuit that recognizes the occurrence of the sequence of bits 1101 on input X by making output Z equal to 1 when the previous three inputs to the circuit were 110 and current input is a 1.
Use clocked D flip-flops. Draw the circuit diagram. What will happen if your counter starts in an invalid state?

Q7. Design a counter that counts in the sequence: 000, 010, 001, 100, 011, 110, 000, ...
Use clocked T flip-flops. Design your counter to go to state 000 from all invalid states. There is no need to draw a circuit diagram.

Q8. The state diagram for a Mealy style clocked sequential network investigates an input sequence X and will produce an output Z=1 for ay input sequences ending in 1101 or 011

Example:

X = 0 0 1 1 0 1 1 0 1 0 1 1 0 1 0
Z = 0 0 0 1 0 1 1 0 1 0 0 1 0 1 0

Q9. A 1-block is a consecutive sequence of 1s bounded on the left by 0 or by the left end of the sequence. Design a state table for a clocked sequential state machine that investigates an input sequence and will produce an output Z = 1 coincident with an input X = 0 that terminates a 1-block of even length (containing an even number of 1s).

Example:
X = 1 1 0 1 1 1 0 0 1 0 0 0 1 1 0 1 1 1 1 0 1 0
Z = 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0