Objective : Simulation of basic building blocks of digital circuits in Verilog using Iverilog/ModelSim simulator

1. Write a verilog code for the D flipflop (with and without synchronous reset). Simulate your verilog model using Modelsim.

2. Write the verilog code for a JK Flip flop, and its testbench. Use all possible combinations of inputs to test its working.

3. Write the hardware description of a 4-bit PRBS (pseudo-random Binary sequence) generator using a linear feedback shift register and test it. The way it is implemented is as given in

   http://en.wikipedia.org/wiki/Linear_feedback_shift_register

   Please bear in mind that you have to make just a 4-bit PRBS generator. You are free to choose your own polynomial for the generator.

4. Write the hardware description of a 8-bit register with shift left and shift right modes of operation and test its operation.

5. Write the hardware description of a 4-bit mod-13 counter and test it.