Estimation of optimal value of optical buffer length for variable length packet under various conditions

Rajat Kumar Singh[*a], Yatindra Nath Singh[b]
[a,b]Dept. of Electrical Engineering, Indian Institute of Technology, Kanpur, UP, INDIA 208016

ABSTRACT

Future optical core networks will be using optical packet switching to transport very high speed aggregate of data. In the optical packet switches for these networks, optical buffering will play an important role to resolve the output contentions of the packets. The difficulty in implementing fully functional photonic equivalents of electronic random access memory (RAM), for optical buffering, makes clocked optical buffering and synchronization more difficult. One possible approach is to use fiber delay lines (FDL), which can be used either in recirculating or traveling configuration. The length of these delay lines can be multiple of fundamental length (D), which is equal to the packet length assuming packets of fixed length. This paper analyzes the optical buffers used for asynchronous and variable length packets and studies the variation of length of optimal (basic) delay unit under different conditions of arrival rates and traffic loads.

Keywords: Optical packet switching, optical buffering, contention.

1. INTRODUCTION

Optical fibers are replacing cables as the transmission media in most long and short-haul communication networks, using optical packet switches. Optical buffering is fundamental to many optical packet switch implementation. Buffering of packets somewhere within the switch is needed to prevent packet contention. When two (or more) packet contend for the same output link, one is transmitted and the other(s) is (are) sent to a coil of fiber to be delayed by an amount of time sufficient to resolve the contention. Dimensioning of the FDL buffers as well as contention resolution techniques in this scenario have been widely studied in the last few years[1-5]. But, when we consider the case of variable length packets, the question arises that what changes should be done. Very little work[6,7] has been devoted to the problem of dimensioning FDL buffers in this case. This paper is extension of the work done by *Callegati*[7]. We have used a simulation model consisting of single queue and single server. This model is valid for output queued switch. For the buffering system, the simulations have been carried out using matlab and the loss probabilities for different cases of arrival rate have been computed and the results are compared.

2. FDL BUFFER AND VARIABLE LENGTH PACKETS

A switching matrix with output queuing is considered assuming that each input and output fiber carries only one wavelength. The buffers have been assumed to follow FCFS scheduling policy. Therefore the queuing system has a single server. It is also assumed the FDLs introduce delays that are consecutive multiple of D μs. In a buffer made with 'B' FDLs, the first delay line introduce a delay of 0 μs, the second, of D μs, the third, of 2D μs and the Bth, a delay of D_M = (B-1)D μs. But for our case of variable length packet, we have to find a suitable value of D known as D_0. Firstly, let us analyze in some detail, how the FDL buffer works. If a packet arrives and finds the server idle, it is served immediately. When a packet arrives and finds the server busy or other packets are queued, it is buffered (or delayed). Assuming the new packet arrives at time t, and the server will be free at time t_f to serve the new packet. Hence the new packet should be delayed by an amount $t_f - t$. Now we have to check for equivalent length of delay line in terms of D for this amount of time. Thus, the new packet will be delayed by an amount,

$$\Delta = \left\lceil \frac{t_f - t}{D} \right\rceil D$$

[*] rajatks@iitk.ac.in; phone +91-9415074431

Where $\lceil x \rceil$ indicates the smallest integer greater than or equal to *x*. Thus, for the time interval $\tau = [\Delta - (t_f - t)] \geq 0$, the output line is not used even when a packet is available to be transmitted. Here it is assumed that the arrival process is independent of the state of the queue and that the lengths of consecutive packets are also independent. Means, when a new packet arrives and has to be queued, 'τ' may take any value between 0 and D with uniform probability, therefore its average value is D/2.

For a given value of B, there must be an optimal value for D because (i).if D is very small, the time resolution of the FDL buffer is high but the buffering capacity is very small and (ii).if D is very large, the buffering capacity is large, but the time resolution of the buffer is very small. Hence there will be a trade-off between time resolution and amount of delay achievable to get a minimum packet loss. Improving upon the previous work [7], the optimal value of D under various condition of arrival rate λ is investigated by us. The mathematical equations that are used for simulation have been taken from *Callegati* [7].

3. NUMERICAL RESULTS & CONCLUSIONS

In the previous work, several graphs are shown for packet loss probability to find out the optimal value (D_0) of FDL for different values of number of buffer (B) and the load (ρ). In this paper, we had compared the optimal value of FDL for different condition of arrival rate by keeping both B & ρ constant in each case for their different values. Few results are shown here. Theoretically, when we will increase the arrival rate, excess load on the system will increase which in turn leads to a smaller desirable value of the fundamental length of FDL (D_0), to compensate the increase of arrival rate. These results (Fig. 1), which is compared for different arrival rates of λ=0.5 & λ=0.75 by keeping B=256 and ρ=0.8, indicates that minimum probability of loss occurs for smaller value of D_0 when arrival rate is higher. The results (Fig. 2) are compared for the λ=0.5 & λ=0.75 at B=256 but this time at higher load ρ=0.9. Again we found the same trend in D_0 for minimal loss probability. The results (Fig. 1 & 2) can also be compared for different load by keeping arrival rate fixed. Here with the increase of the load ρ, Loss probability will be minimal for the smaller value D_0, which is desired analytically. We had also compared the excess load for two different cases of arrival rate and same load ρ. The results (Fig. 3 & 4) indicate that with the decrease in the arrival rate, for same ρ (0.8 & 0.9), the excess load on the system also go down, which follows the theoretical analysis.

One can concludes that if a switch has to be designed to operate at higher arrival rate with moderate load, then the length of the fundamental buffer (D_0) as well as the total number of buffers (B) should be considered appropriately. Value of B is also a key factor and must be chosen correctly.

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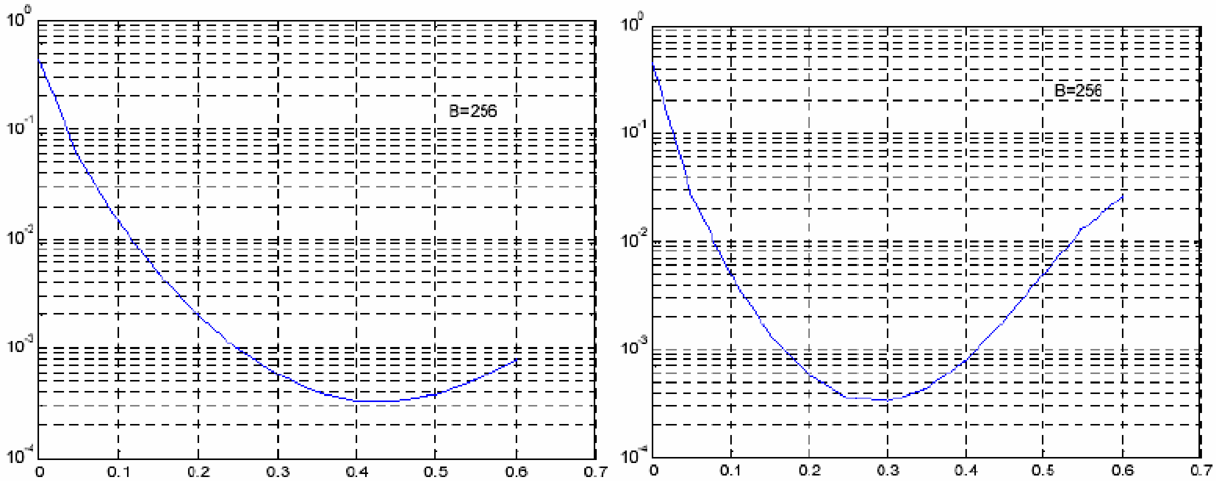

Figure 1: Comparison of ‘Probability of Loss’ Vs D, for two different arrival rate, λ=0.5 & λ=0.75 and B=256 at ρ=0.8.

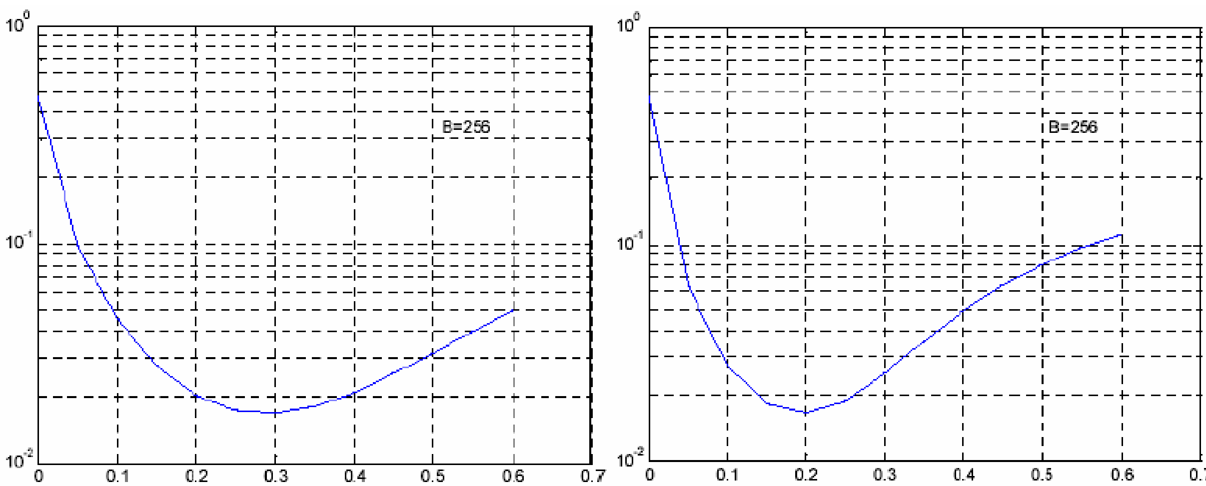

Figure 2: Comparison of ‘Probability of Loss’ Vs D, for two different arrival rate, λ=0.5 & λ=0.75 and B=256 at ρ=0.9.

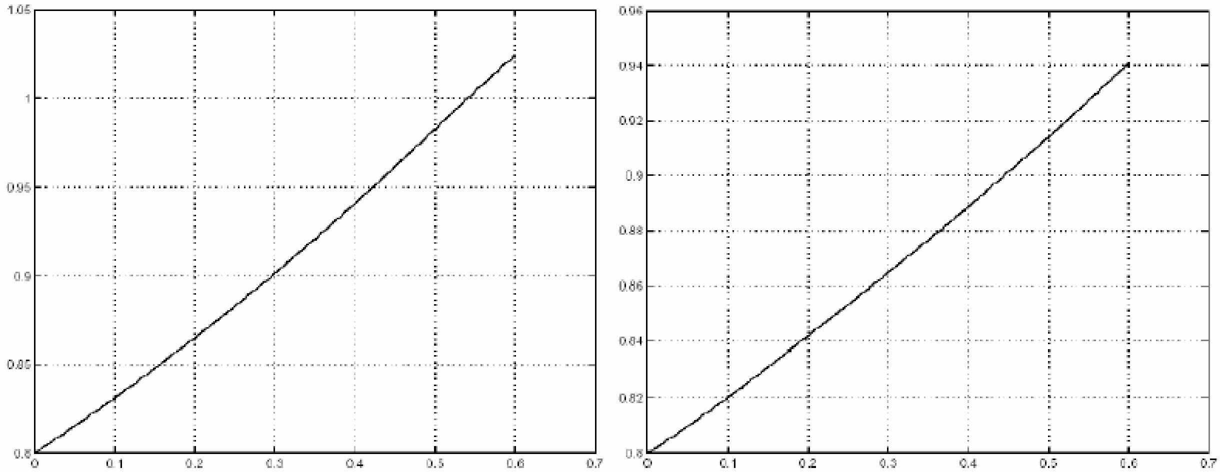

Figure 3: Comparison of 'Excess load' Vs D for arrival rate of λ=0.75 & λ=0.5 at ρ=0.8.

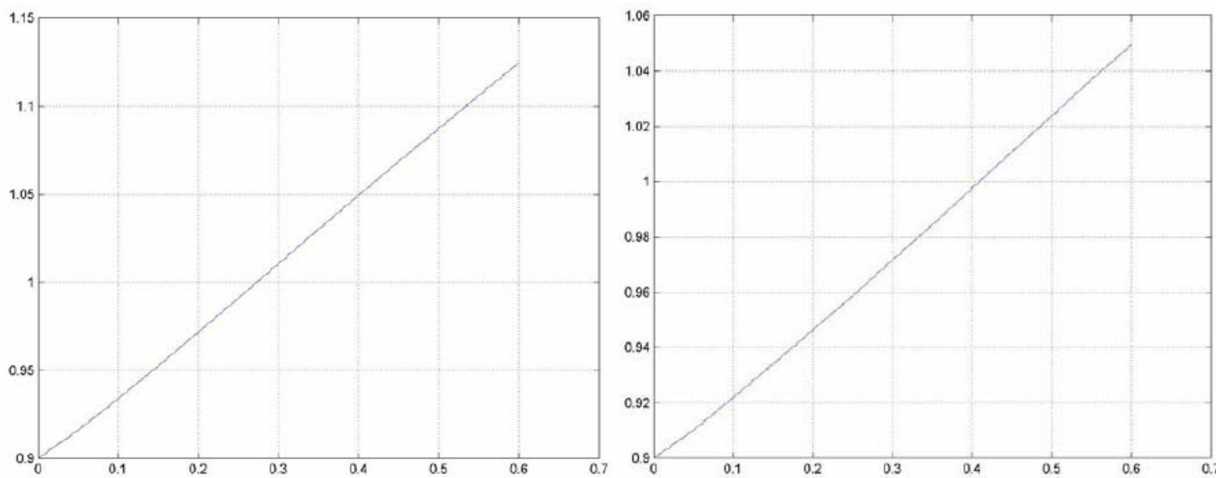

Figure 4: Comparison of 'Excess load' Vs D for arrival rate of λ=0.75 & λ=0.5 at ρ=0.9.