Design and Implementation of Combinational Circuits using Verilog

Aim :

1. **Structural and data flow coding of the design in Verilog as a module**
2. **Behavioural coding of a Verilog test bench to test the designed module**

Assignment statement

To design and implement the following combinational circuit using data flow or gate level modelling along with their test bench :

a. Basic gates
b. 2:1 and 4:1 Multiplexer (consider using 2-bit inputs and outputs)
c. 3:8 Decoder (consider using 4-bit inputs and outputs)
d. 2- bit magnitude comparator
e. 8:3 encoder

f. Design an excess-3 to seven segment decoder for a common anode LED display.

Inputs will be 4-bit excess-3 coded decimal digits; seven low active output lines will drive the corresponding seven segments of the common anode LEDs.

Each of the seven functions corresponding to the seven outputs should be minimised using Karnaugh's maps. Common terms among the functions may be shared to avoid duplication.

Next, encode the design in Verilog as a module and also write a suitable behavioral test bench module. Simulate the design using the Verilog simulator available.

Instructions for submission :

Submit your codes (the verilog dsign and testbench files properly named according to the design zipped in a folder named $$_lab1 , where $$ will be your roll no.) at the end of the class to systemlab.iiita@gmail.com