

Title : Power Aware Compiler for Embedded Processors

I. ABSTRACT

As embedded systems are becoming more computationally intensive, power consumption has gained importance vis-a-vis performance. Software based control of different components in embedded devices has paved the way for development of compilation and operating strategies to reduce power dissipation in these devices. However, research suggests that majority of low power optimization techniques have been by-product of performance optimizations. In this work, we wish to explore different compiler based optimization techniques specifically targeting low power embedded devices and then develop these techniques as libraries which can be integrated in any compilation flow for embedded systems. Next, each of the considered technique would be evaluated for its benefit by performing physical measurements on different target systems for a set of representative benchmarks. Finally, we plan to integrate the developed libraries in LLVM compiler infrastructure framework to provide a complete power aware compiler solution for embedded device
